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EXAMINER	
TO, JENNIFER N	
ART UNIT	**PAPER NUMBER**
2195	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/651,381	MEHTA, KALPESH D.	
	Examiner	Art Unit	
	JENNIFER N. TO	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-10 rejected under 35 U.S.C. 101 because the cited claims are non-statutory. The recited claims are directed toward an apparatus comprising a plurality of blocks wherein all of which are conceivably software and/or software constructs. Therefore, the cited apparatus comprising a plurality of software constructs without any associated hardware and are considered software per se, such that it does not fit the statutory category of a machine. In addition, the software is not stored on a computer storage medium that would make the functions of the software realized.

> 35 U.S.C. 101 defines four categories of inventions that Congress deemed to be the appropriate subject matter of a patent: processes, machines, manufactures and compositions of matter. The latter three categories define "things" or "products" while the first category defines "actions" (i.e., inventions that consist of a series of steps or acts to be performed). See 35 U.S.C. 100(b) ("The term process' means process, art, or method, and includes a new use of a known process, machine, manufacture, composition of matter, or material.")

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over MOTOMURA (U.S. Patent 5,815,727).

4. MOTOMURA was cited in the previous office action.

5. As to claim 1, MOTOMURA teaches an apparatus comprising: a storage block (thread descriptor storage device) (fig. 1; col. 3, lines 12-50; col. 3, lines 55-64); an execution block to execute threads (via the processor executing the threads / ordered multithread executing system) (fig. 1; col. 3, lines 12-50; col. 3, lines 55-64); and a thread management block (thread descriptor ordering system / ordered multithread executing system) (fig. 1) coupled to the storage and execution blocks, and equipped to store and maintain a thread switching structure (stack / array of virtual thread numbers of threads for execution) in the storage block to facilitate interleaving execution of a plurality of threads by the execution block (col. 2, lines 44-60; col. 3, lines 12-50; col. 3, lines 55-64), with the thread switching structure including a current thread identifier (virtual thread numbers) identifying one of the plurality of threads as a current thread being currently executed by the execution block (via being the lowest virtual thread number / via executing a thread which inherently would identify the thread as executing by the processor) (col. 5, lines 5-56; col. 8, lines 13-51), and a thread array of thread entries (stack / array of virtual thread numbers of threads that are spawned for execution), one per thread, correspondingly describing the plurality of threads (via the

forked command), each thread entry being created and added to the thread array by the thread management block as part of the execution of a create thread instruction (fork command) of a thread to spawn execution of another thread (via when a processor forks other threads during execution of a certain thread, a fork demand is transferred to the ordered multithread executing system and a thread descriptor is fed to the ordered multithread executing system) (col. 8, lines 13-51). However, MOTOMURA does not teach that the execution of instructions from threads by the thread management block. MOTOMURA does teach the execution of threads (abstract). Official Notice is taken in that it is well known in the art that threads are made up of instructions and that it would be obvious to one of ordinary skill in the art that by executing the threads, one is executing the instructions of the threads and therefore obvious that the instructions of threads are interleaved since threads are executed and interleaved by some a scheduling routine.

6. As to claim 2, MOTOMURA teaches each thread entry (thread descriptors stored for a forked thread) comprises a thread pointer counter to identify an instruction of the corresponding described thread as a current instruction to be executed, when the corresponding described thread is being executed (via the thread descriptor which is stored in the thread descriptor storage device comprises a start instruction address of the thread) (col. 8, lines 35-39).

7. As to claim 3, MOTOMURA teaches each thread entry comprises an activeness indicator (state indication of executable or waiting) indicating whether the corresponding described thread is currently in an active state (executable) or an inactive state (waiting), where the corresponding described thread is to be included among the threads to be interleaving executed by the execution block, while the thread is in the active state, and not included, while the thread is in the inactive state (via storing virtual thread numbers with the threads such that the threads are executed based on the lowest virtual thread number and threads in the waiting state are not present or selected for executions since all executable threads have lower virtual thread numbers) (col. 9, lines 42-67; col. 10, lines 1-5; col. 10, lines 15-56).

8. As to claim 4, MOTOMURA teaches the thread management block is equipped to reset the activeness indicator of a thread from the active state to the inactive state, as part of the execution of a thread termination instruction of at thread terminating its own execution (via the thread being no longer executable, and is removed from the stack / array of thread descriptors and thereby reset when it terminates) (col. 15, line 27 - col. 16, line 27).

9. As to claims 5 and 6, MOTOMURA teaches each thread entry comprises thread dependency information describing information on which the corresponding thread depends for execution (col. 8, lines 35-39). MOTOMURA also teaches that each thread is loaded and executed by processors (col. 9, lines 42-67). However, MOTOMURA

does not explicitly mention that the information describes registers used by the threads. Official Notice is taken in that a thread state includes register information and that when a thread is switched in and switched out for execution that its register information is saved and restored also. Therefore, it is obvious to the teachings of MOTOMURA that the dependency information describes the register information such that the register information is loaded when the thread is loaded for execution.

10. As to claim 7, MOTOMURA teaches loading threads into processors for execution such that they are the current threads executing (col. 9, lines 42-67). It is inherent from this teaching that the program counter for the processor is updated as threads are switched in and switched out to be the current thread for execution.

11. As to claim 8, MOTOMURA teaches the execution block is equipped to select the next current thread on a selected one of a round-robin basis, a fixed priority basis, and a rotating priority basis (via selecting based on the lowest virtual thread number / priority) (col. 10, lines 34-47; col. 10, lines 57-64).

12. As to claim 9, MOTOMURA teaches the ordered multithreaded executing system is a parallel processor system having processor interfaces to respective processors (col. 11, lines 1-19). Therefore, MOTOMURA teaches the processing block having an input / output interface and configured as an input interface when sending commands / threads

to the processors and an output interface when receiving responses / results from the processors.

13. As to claim 10, MOTOMORA teaches the thread descriptors have a pointer to the arguments (col. 8, lines 35-39). Therefore, it would be inherent that there exists another storage block to store data of the threads.

14. As to claims 11-17, reference is made to a method that corresponds to the block of claims 1-10 and is therefore met by the rejection of claims 1-10 above.

15. As to claims 18-23, refer to claims 1-10 for rejection. Claims 18-23 further details the recited block is coupled to a set of registers and includes an interface with the capability of performing mathematical operations. MOTOMURA teaches the ordered multithreaded executing system is a parallel processor system having processor interfaces to respective processors (col. 11, lines 1-19). MOTOMURA also teaches that each thread is loaded and executed by processors (col. 9, lines 42-67). However, MOTOMURA does not explicitly mention that the information describes registers used by the threads. Official Notice is taken in that a thread state includes register information and that when a thread is switched in and switched out for execution that its register information is saved and restored also. Therefore, it is obvious to the teachings of MOTOMURA that the dependency information describes the register information such that the register information is loaded when the thread is loaded for execution. In

addition it is well known to one of ordinary skill in the art that mathematical operations are a form of thread operations and that the threads executed by the processors of MOTOMURA perform mathematical operations since such operations within threads are well known in the art.

16. As to claims 24-29, refer to claims 18-23 above for rejection. However, claims 24-29 further detail a media processor comprising a DMA unit and a plurality of signal processing units coupled to the DMA unit to process the accessed media data. MOTMOMURA teaches the parallel processing system includes an arbitrary number of processors and a multithread executing system common to the processors and a memory device connected to the processors (col. 8, lines 1-12). It is obvious to one of ordinary skill in the art that the ordered multithread executing system is the media processor, the memory device is the DMA unit, and the number of processors is the signal processing units coupled to the DMA unit to process the data / threads.

17. As to claims 30-36, refer to claims 24-29 for rejection. However, claims 30-36 further detail a host processor having first memory, a media processor having second memory / DMA unit and a plurality of signal processing units coupled to the DMA unit to process the accessed media data. MOTMOMURA teaches the parallel processing system includes an arbitrary number of processors and a multithread executing system common to the processors and a memory device connected to the processors (col. 8, lines 1-12). It is obvious to one of ordinary skill in the art that the ordered multithread

executing system is the media processor, the memory device is the DMA unit, and the number of processors is the signal processing units coupled to the DMA unit to process the data / threads. In addition, since the recited claims provide no functional interaction between the host processor and the media processor, except for a connection, it would be obvious to one of ordinary skill in the art that a well known master processor chip is associated with the multithreaded executing system since the invention allows for less important and known elements are part of the invention (col. 8, lines 1-12; col. 24, lines 46-56).

Response to Arguments

18. Applicant's arguments filed 04/01/2008 have been fully considered but they are not persuasive.

19. In the remark, applicant argued that:

(1) MOTOMURA fails to teach an execution block to execute instructions provided from a thread switching structure maintained by a thread switching block;

(2) MOTOMURA fails to teach an I/O interface configured to be a selected one of an input and output interface;

(3) MOTOMURA fails to teach an indicator indicate a thread is inactive; and

(4) MOTOMURA fails to teach utilizing the various processors for specialized tasks, such as input, output, or computation.

20. Examiner respectful disagreed with applicant.

As to point (1), MOTOMURA teaches an execution block to execute instructions provided from a thread switching structure maintained by a thread switching block (via the processor executing the threads / ordered multithread executing system) (fig. 1; col. 3, lines 12-50; col. 3, lines 55-64); and a thread management block (thread descriptor ordering system / ordered multithread executing system) (fig. 1). Although MOTOMURA teaches more than one processors in the system but according to MOTOMURA each processor (i.e. execution block) executes instructions provided from a thread switching structure maintained by a thread switching block. In addition, the claim language recited “comprising”, thus it is an open ended statement, therefore the claim language not just narrow to only one processor in the system as argued by applicant. Therefore, MOTOMURA clearly teaches an execution block to execute instructions provided from a thread switching structure maintained by a thread switching block. Examiner suggested applicant to amend the claim to include the language of "consisting" a single execution block in order to be interpreted the claim as an apparatus having only processor.

As to point (2), MOTOMURA teaches an I/O interface configured to be a selected one of an input and output interface (col. 11, lines 1-19; each processor have a respective interface, thus MOTOMURA’s system teaches each processor having an input / output interface and configured as an input interface when sending commands /

threads to the processors and an output interface when receiving responses / results from the processors).

As to point (3), MOTOMURA teaches an indicator indicate a thread is inactive (col. 15, line 27 - col. 16, line 27). Although the thread is in active accordance to MOTOMURA is a thread in waiting state, but it is still meet the language of the recited claim because the recited claim language did not recite that the thread is inactive meaning that the thread is completely terminate for execution and removed from the queue as argued by applicant.

As to point (4), argued that MOTOMURA fails to teach utilizing the various processors for specialized tasks, such as input, output, or computation) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure (see PTO form 892 for details).

22. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

23. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JENNIFER N. TO whose telephone number is (571)272-7212. The examiner can normally be reached on M-T 6AM- 3:30 PM, F 6AM- 2:30 PM.

25. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

26. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

Jennifer N. To
Examiner
GAU 2195